**Joint Group on Pollution Prevention**
**(JG-PP)**

# Joint Test Protocol
# J-01-EM-026-P1

# for Validation of Alternatives to Eutectic Tin-Lead Solders used in Manufacturing and Rework of Printed Wiring Assemblies

**February 14, 2003**
**(Revised April 2004)**

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## PREFACE

This report was prepared on behalf of, and under guidance provided by, the Joint Group on Pollution Prevention (JG-PP) through the JG-PP Working Group. The structure, format, and depth of the report's technical content were determined by the Working Group, government technical representatives, and government contractors in response to the specific needs of this project.

Invaluable technical, business, and programmatic contributions were provided by the organizations listed below.

- Aging Aircraft Avionics
- Air Force Research Laboratory/MLSA, Wright Patterson AFB
- American Competitiveness Institute
- AMKOR
- Astrium Space (U.K.)
- ATK Thiokol
- BAE Systems (U.K.)
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- Celestica
- Corfin Industries
- Ensil International Corporation (Canada)
- European Space Agency
- F-15 Program Office
- Florida Cirtech
- Hanscom Air Force Base
- Harris
- Heraeus
- Hill Air Force Base
- Honeywell
- HQ Defense Contract Management Agency
- HQ-AFMC/LG-EV, Wright Patterson Air Force Base
- Indium Corporation
- International Trade Bridge, Inc.
- Intersil
- ITT
- F-35 Joint Strike Fighter
- Lockheed Martin
- MBDA (U.K.)
- Mitsui Comtek/Senju Metals Co.
- NASA Ames Research Center
- NASA Goddard Space Flight Center
- NASA Jet Propulsion Lab

- NASA Marshall Space Flight Center
- NASA Space Shuttle Main Engine (SSME) Program
- National Center for Manufacturing Sciences
- National Institute of Standards and Technology
- Naval Air Systems Command
- Naval Air Warfare Center - Weapons Division
- Naval Sea Systems Command
- Northrop Grumman
- Office of Chief of Naval Operations, Environmental Protection, Safety, and Occupational Health
- Randolph Air Force Base
- Raytheon
- Redstone Army Arsenal
- Rockwell Collins
- Sandia Labs
- Senju Solder - Mitsui
- Texas Instruments
- Tinker Air Force Base
- TRW/ICBM
- U.S. Army Aviation and Missile Command
- U.S. Army Communications-Electronics Command
- U.S. Army Tank-Automotive and Armaments Command; Armament Research, Development and Engineering Center
- U.S. Marine Corps Materiel Command
- U.S. Marine Corps Systems Command
- United Defense Limited Partnership
- United Space Alliance – Solid Rocket Boosters
- Vitronics-Soltec
- Warner Robins Air Logistics Center, Robins Air Force Base

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## ACRONYMS

| | |
|---|---|
| AMCOM | U.S. Army Aviation and Missile Command |
| ANSI | American National Standards Institute |
| ATS | Automated Test Set |
| BGA | Ball Grid Array |
| CET | Combined Environments Test |
| CSP | Chip Scale Package |
| CTE | Coefficient of Thermal Expansion |
| dB | Decibel |
| DoD | Department of Defense |
| DOF | Degrees Of Freedom |
| EDX | Energy Dispersive X-Ray |
| EEE | Electronic, Electrical and Electromechanical |
| EIA | Electronic Industries Association |
| EPA | Environmental Protection Agency |
| $g_{rms}$ | Acceleration of Gravity, root mean square |
| GF | Glass Fiber |
| HALT | Highly Accelerated Life Test |
| HASL | Hot Air Solder Leveled |
| Hz | Hertz |
| IPC | Institute of Printed Circuits |
| JG-PP | Joint Group on Pollution Prevention |
| JLC | Joint Logistics Commanders |
| JTP | Joint Test Protocol |
| JTR | Joint Test Report |
| MIL | Military |
| NAWC | Naval Air Warfare Center |
| $^{o}C$ | Degrees Celsius |
| oct | Octave |
| OEM | Original Equipment Manufacturer |
| $^{o}F$ | Degrees Fahrenheit |
| PDIP | Plastic dual-in-line package |
| PTH | Plated Through Hole |
| PWA | Printed Wiring Assembly |
| RH | Relative Humidity |
| SM | Surface Mount |
| SMT | Surface Mount Technology |
| Sn63 | Eutectic tin-lead solder alloy |
| SnAgCu | Tin-Silver-Copper solder alloy |
| SnAgCuBi | Tin-Silver-Copper-Bismuth solder alloy |
| SRS | Shock Response Spectrum |
| SSME | Space Shuttle Main Engine |
| STD | Standard |
| TACOM-ARDEC | U.S. Army Tank-Automotive and Armaments Command; Armament Research, Development and Engineering Center |
| Tg | Glass Transition Temperature |
| TM | Technical Manual |
| TQFP | Thin Quad Flat Pack |
| TSOP | Thin Small Outline Package |
| XRF | X-Ray Fluorescence |

# 1. INTRODUCTION

On September 15, 1994, the Joint Logistics Commanders (JLC) chartered the Joint Group on Pollution Prevention (JG-PP) to coordinate joint service activities affecting pollution prevention issues identified during a defense system's acquisition process. JG-PP's primary objectives are to:

- Reduce or eliminate the use of hazardous materials (HazMats) by fostering joint cooperation
- Avoid duplication of efforts in actions required to reduce or eliminate HazMats and share technology.

JG-PP focuses on implementing pollution prevention processes at defense contractor design, manufacturing, and re-manufacturing locations, with subsequent technology transfer to the U. S. Department of Defense (DoD) Sustainment Community. JG-PP is managed by the JG-PP Working Group.

The JG-PP Working Group has developed a methodology for implementing pollution prevention processes through interactions with original equipment manufacturers (OEMs) at several defense contractor locations. The JG-PP methodology is being used by the Lead-Free Solder project team with the intent of facilitating the team's efforts to identify and use environmentally acceptable materials and processes for circuit card manufacturing and maintenance.

## 1.1. Lead-Free Solder Overview

The use of conventional tin-lead (Sn-Pb) solder in circuit board manufacturing is under ever-increasing political scrutiny due to environmental issues and increasing regulations concerning lead. Lead and lead compounds have been cited by the EPA as one of the top 17 chemicals imposing the greatest threat to human health. The European Union's recently enacted "Restriction of Hazardous Substances" (RoHS) directive and a pact between the U.S. NEMI, Europe's Soldertec at Tin Technology Ltd. and Japan's JEITA are just two examples where worldwide legislative actions and partnerships/agreements are impacting the electronics industry. As a result many global commercial grade electronic component manufacturers are initiating efforts to retain their worldwide market. These components will be finding their way into the inventory of aerospace or military assembly processes under government acquisition reform initiatives. These actions will result in increased risks associated with manufacturing and subsequent repair of military electronic systems.

Starting in CY2001, U.S. EPA lowered the Toxic Release Inventory (TRI) reporting threshold for lead to 100 pounds annually. Previously, facilities were not required to report releases of lead and lead compounds unless they manufactured or processed more than 25,000 pounds annually, or use more than 10,000 pounds a year. This requirement

impacts Federal facilities, which, under Executive Order 12856, must file annual Toxic Release Inventory reports if they meet the threshold requirements.

The commercial sector is driving component and board suppliers to provide primarily lead-free compatible surface finishes and alloys. If the military electronics industry does not proactively participate in determining the impact of lead-free solders, it is possible that parts with lead or Sn-Pb finishes may become impossible to procure or acquisition costs for "military lead containing components" will become prohibitive. The military and space sectors need to become an active participant in addressing the issue or it may quickly be perceived as a part of the problem.

Since military and space applications typically are more severe than traditional commercial electronic applications the JG-PP Lead-Free Solder project has been established. The purpose of the Lead-Free Solder JG-PP project is to characterize, demonstrate and validate the performance of lead-free solders as potential replacements of conventional tin-lead solders used on circuit card assemblies. This project's focus will be on lead-free solders for use on plated through hole (PTH), surface mount technology (SMT), and mixed technology circuit card assembly applications.

## 1.2. Project Approach

A joint group led by the JG-PP Working Group and project technical representatives identified engineering, performance, and operational impact (supportability) requirements for circuit card assemblies manufactured and reworked with lead-free solder alloys. The joint group consisted of technical representatives from the affected defense and space programs, DoD Sustainment Community, and other government and contractor organizations. The joint group reached consensus regarding the tests, procedures, methodologies and acceptance criteria to qualify alternatives against the requirements.

This Joint Test Protocol (JTP) contains critical technical and performance requirements and tests agreed to by the joint group for use on DoD circuit cards. These requirements are at least the first step to validate the performance and reliability of circuit card assemblies, manufactured and reworked, with lead-free solder alloys.

The JG-PP Working Group and project technical representatives selected rework procedures over repair procedures for the JG-PP Lead-Free Solder testing program based on the following descriptions.

- *Rework;* The act of reprocessing non-complying articles, through the use of original or equivalent processing, in a manner that assumes full compliance of the article with applicable drawings or specifications.
- *Repair;* The act of restoring the functional capability of a defective article in a manner that precludes compliance of the article with applicable drawings or specifications.

A subsequent Joint Test Report (JTR) will document the data and results of testing. The JTP and JTR will be made available to other government and commercial users for guidance on future pollution prevention efforts. Engineering authorities can refer to the lead-free solder alloy test results during design decisions for specific defense and space systems. However, the tests and criteria defined in this JTP were developed by consensus only for the defense and space system programs involved, and may not address all areas of application. A list of some of the potentially affected defense, space, and aerospace equipment and platforms are included in Appendix A.

Table 1 is a summary table, which shows the target HazMats, current, processes, applications, and current specifications affected by this JG-PP project.

**Table 1. Target HazMat Summary**

| **Target HazMats** | **Current Processes** | **Applications** |
|---|---|---|
| Lead | Soldering<br>• Wave<br>• Reflow<br>• Manual | Electrical interconnects |
| **Current Specifications** | | |
| IPC/EIA J-STD-001 Revision C | IPC-SM-785 | IPC-TM-650 |
| ANSI/J-STD-003 | IPC-9201 | IPC-9701 |
| IPC-2221 | MIL-STD-810F | IPC-A-610 |
| IPC-2222 | | IPC-6012 |

## 2. ENGINEERING AND TESTING REQUIREMENTS

This section summarizes the engineering and testing requirements for circuit cards prepared with lead-free solder alloys. Tests contained in this JTP may involve the use of hazardous materials. However, this JTP does not address safety issues associated with their use. Therefore, when performing tests described in this JTP, appropriate safety and health practices must be established, and the applicability of regulatory limitations must be determined.

### 2.1. Test Vehicle- Printed Wiring Assembly

The test vehicle for most tests in this JTP (except where noted) is a printed wiring assembly (PWA), designed to evaluate solder joint reliability. Test vehicle raw boards shall comply with IPC-6012, Class *3* (*Qualification and Performance Specification for Rigid Printed Boards*). The design incorporates components representative of the parts used for defense and space systems and is designed to reveal relative differences in solder alloy performance. The test vehicle will be used for all tests except Surface Insulation Resistance, JTP Section 3.3.3 and Electrochemical Migration Resistance Test, JTP Section 3.3.4.

The test vehicle will include a variety of plated through hole (PTH) and surface mount technology (SMT) components. All components will be dummy daisy-chained components and will contain simulated die. The circuit board will be designed with daisy-chained pads that are complementary to the daisy chain in the components, except for the chip capacitors. Therefore, the solder joints on each component will be part of a continuous electrical pathway that can be monitored during testing by an event detector (Anatech or equivalent). Failure of a solder joint on a component will break the continuous pathway and be recorded as an event. Each component will have its own distinct pathway (channel).

#### 2.1.1. Test Vehicle for Manufactured PWAs

##### 2.1.1.1. Lead-Free Assembly of Manufactured PWAs

The lead-free printed wiring boards shall have an immersion silver surface finish; be made from high temperature laminate (glass transition temperature of 170 $^{o}$C per IPC-4101/26); and components will be attached using the alternative lead-free solder alloys (see Table 2). Processing procedures for the lead-free assembly of manufactured printed wiring boards is outlined in Appendix B.

##### 2.1.1.2. Baseline Assembly of Manufactured PWAs

The baseline (control) printed wiring board shall have an immersion silver surface finish; be made from high temperature laminate (glass transition temperature of 170 $^{o}$C per IPC-4101/26); and components will be attached using eutectic tin lead solder (see Table 2). Processing procedures for the baseline assembly of manufactured PWAs are outlined in Appendix B.

**Table 2. Test Vehicle Matrix for Manufactured PWAs**

| Type | Laminate [a] | Surface Finish | Reflow Solder | Wave Solder |
|---|---|---|---|---|
| Lead-Free Manufactured | High Tg, FR4 | Immersion Silver | Tin-Silver-Copper | Tin-Silver-Copper |
| | | | Tin-Silver-Copper-Bismuth | Tin-Copper |
| Baseline (control) | High Tg, FR4 | Immersion Silver | Eutectic Tin-Lead | Eutectic Tin-Lead |

### 2.1.2. Test Vehicle for Reworked PWAs

#### 2.1.2.1. Lead-Free Rework of Tin/Lead Assemblies

PWAs reworked using lead-free solder shall have a hot air solder leveled (HASL) surface finish, be made from low temperature laminate (glass transition temperature in the range of 135$^{o}$C to 140$^{o}$C per IPC-4101/21) and initially soldered using eutectic tin/lead solder. The lead-free rework shall consist of removing and replacing the ball grid arrays (BGA), thin quad flat packs (TQFP), thin small outline packages (TSOP) and the plastic dual-in-line packages (PDIP). The components shall be de-soldered from the assembly. The remaining tin/lead solder on the pads shall be solder wicked. New components will be used to replace the removed components and re-soldered using the lead-free solder(s) per Table 3. Processing procedures for lead-free rework of tin-lead assemblies are outlined in Appendix B.

#### 2.1.2.2. Tin/Lead Rework of Tin/Lead Assemblies

The control rework printed wiring assemblies shall have a HASL surface finish, and will be made from low temperature laminate (glass transition temperature in the range of 135$^{o}$C to 140$^{o}$C per IPC-4101/21) and soldered using eutectic tin/lead solder. Once the initial processing is complete, certain components (BGAs, TQFPs, TSOPs and PDIPs) shall be de-soldered from the assembly. The remaining tin/lead solder on the pads shall be solder wicked. New components will be used to replace the removed components and re-soldered using eutectic tin/lead solder per

Table 3. Processing procedures for tin/lead rework of tin-lead assemblies are outlined in Appendix B.

**Table 3. Test Vehicle Matrix for Reworked PWAs**

| Type | Laminate [a] | Surface Finish | Reflow & Wave Solder Alloy | Rework Solder Alloy SMT | Rework Solder Alloy PTH |
|---|---|---|---|---|---|
| Lead-Free Rework | Low Tg, FR4 | Hot Air Solder Leveled (HASL) | Eutectic Tin-Lead | Tin-Silver –Copper-Bismuth[b] | Tin-Copper |
| | | | | Tin-Silver-Copper[b] | Tin-Silver-Copper |
| Rework Control | Low Tg, FR4 | Hot Air Solder Leveled (HASL) | Eutectic Tin-Lead | Eutectic Tin-Lead[b] | Eutectic Tin-Lead |

[b] *A separate set of boards will be prepared for each line in Table 3.*

## 2.2. General Inspection Procedures

### 2.2.1. Pre-Test Inspection

Visual inspection and photographs will document the visual appearance of the solder joints prior to testing. Deviations from IPC/EIA J-STD-001 Revision C, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*) will be noted. X-ray will be used to document solder ball alignment and voiding. Prior to assembly, board finishes and component finishes must be verified by energy dispersive X-ray (EDX) or X-ray fluorescence (XRF). Prior to assembly, a few components of each type should be tested, using an ohmmeter, to make sure that they are daisy-chained internally. A complete inspection log for pre-test inspection is shown in Appendix C.

### 2.2.2. Post-Test Inspection

Visual inspection and photographs will document the visual appearance of the solder joints after testing is completed. One assembled test vehicle per solder will be set aside for cross sections, (3 manufactured test vehicles plus 3 reworked test vehicles), and will not undergo testing. Cross sections will be done to document post-test metallography and measures solder joint height and ball grid array (BGA) and chip scale package (CSP) solder ball alignment. A complete inspection log for post-test inspection is shown in Appendix C.

## 2.3. Common Engineering, Performance, Testing Requirements and Test Flow

The common performance requirements and related tests for PWAs are listed in Table 4. These tests are required by all defense and space systems that

participated in the development of this JTP (as listed in the Preface). Both manufactured and reworked PWAs will be subjected to all common tests.

**Table 4. Common Performance Requirements**

| Validation Test | JTP Section | Reference | Electrical Test | Acceptance Criteria [(a)] |
|---|---|---|---|---|
| Vibration | 3.2.1 | MIL-STD-810F, Method 514.5, Procedure I | Electrical continuity failure | Better than or equal to tin/lead controls |
| Mechanical Shock | 3.2.2 | MIL-STD-810F, Method 516.5 | Electrical continuity failure | Better than or equal to tin/lead controls |
| Thermal Shock | 3.2.3 | MIL-STD-810F, Method 503.4, Procedure I | Electrical continuity failure | Better than or equal to tin/lead controls at 10% Weibull cumulative failures |
| Thermal Cycling | 3.2.4 | IPC-SM-785 | Electrical continuity failure | Better than or equal to tin/lead controls at 10% Weibull cumulative failures |
| Combined Environments Test | 3.2.5 | MIL-STD-810F Method 520.2 Procedure I | Electrical continuity failure | Better than or equal to tin/lead controls at 10% Weibull cumulative failures |

[a] Failure of a test board in a specific test does not necessarily disqualify a lead-free solder alloy for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

The following test flows will be used for executing the common tests; specifically, Figure 1 is the common test flow for manufactured PWAs and Figure 2 is the common test flow for reworked PWAs.

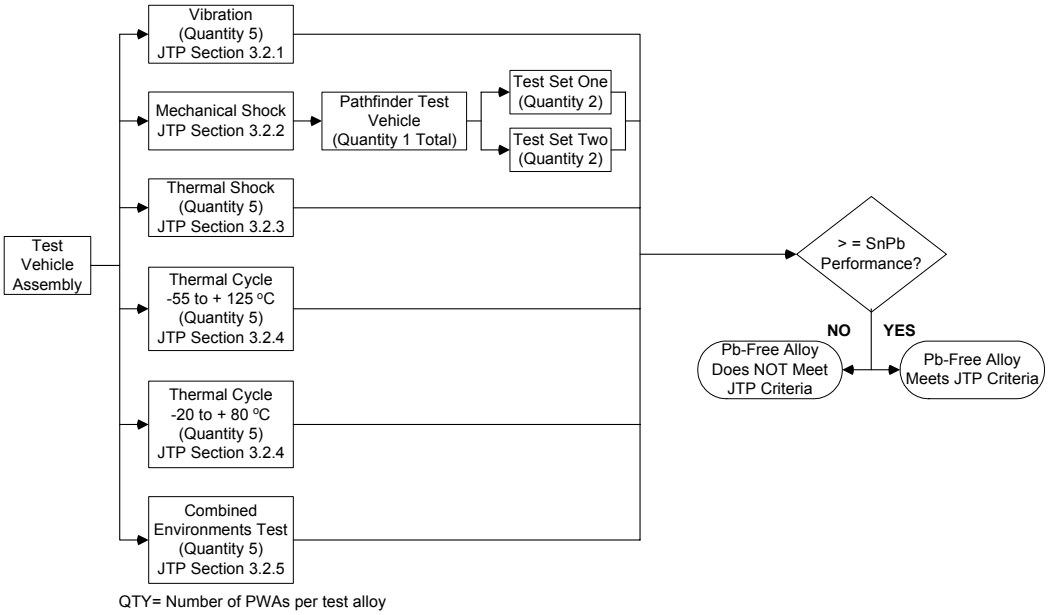



**Figure 1. Common Test Flow Diagram for Manufactured Test Boards**

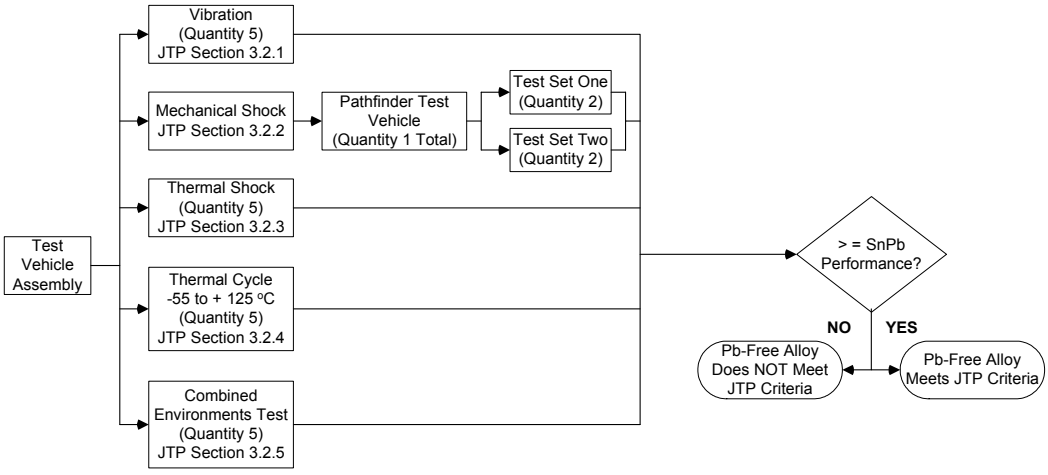



**Figure 2. Common Test Flow Diagram for Rework Test Boards**

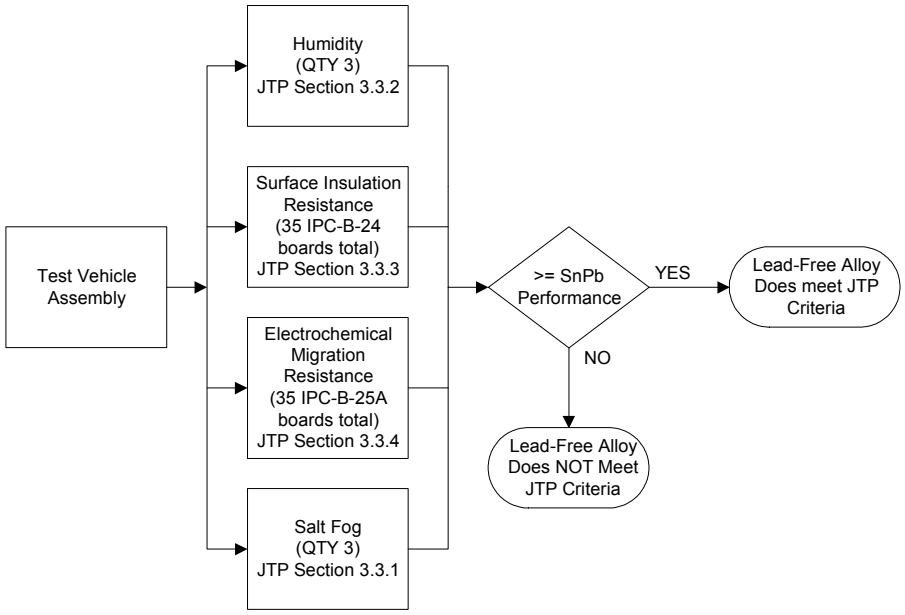
## 2.4. Extended Engineering, Performance, Testing Requirements and Test Flow

The extended test requirements for validating alternatives for lead-free solders are in Table 5. These tests are in addition to the tests identified in Table 4 and will be performed as needed by specific defense and space systems. For two of the extended tests, Humidity and Salt Fog, the test vehicle is the same as described in Section 2.1. However, for the Surface Insulation Resistance and Electrochemical Migration test, a standard IPC test board will be used.

**Table 5. Extended Performance Requirements**

| Validation Test | JTP Section | Reference | Measurement | Acceptance Criteria [a] |
|---|---|---|---|---|
| Salt Fog | 3.3.1 | MIL-STD-810F, Method 509.4 | Visual pass/fail criteria per referenced standard | Better than or equal to tin/lead controls |
| Humidity | 3.3.2 | MIL-STD-810F, Method 507.4 | Visual pass/fail criteria per referenced standard | Better than or equal to tin/lead controls |
| Surface Insulation Resistance, Fluxes | 3.3.3 | IPC-TM-650, Method 2.6.3.3 | Resistance Measurements | $\geq 10^8$ ohms (Ω) |
| Electrochemical Migration Resistance Test | 3.3.4 | IPC-TM-650, Method 2.6.14.1 | Visual pass/fail criteria per referenced standard | • $IR_{final} \geq (IR_{initial})/10$<br>• No evidence of electrochemical migration<br>• No corrosion of the conductors |

[a] Failure of a test board in a specific test does not necessarily disqualify a lead-free solder alloy for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.




[a] *QTY=number of PWAs per test alloy*

**Figure 3. Extended Test Flow Diagram for Manufactured Test Boards**

## 2.5 Quality Assurance

Statistical considerations are essential for meaningful conclusions that will hold up under scrutiny. As such, the numbers of components on the test vehicle and the test sample sizes have been selected to provide statistically meaningful results.

Statistical review of the data generated by the testing is of utmost importance to the JG-PP project consortium. Statistical distribution of failures will be represented by a Weibull distribution. As the lead-free solder testing is performed and the solder joints fail, Weibull distribution coefficients will be determined for the data collected as discussed in IPC-9701, section 5.2. The data of most interest is the first solder joint failure; the number of cycles required to reach 63.2% failures (called the characteristic life or alpha); the failure free period; and the Weibull shape parameter (beta).

When one solder joint fails on a component, the whole component is considered failed. In order to generate useful Weibull plots, ideally 50% of the assemblies must fail with a 63.2% component failure rate preferred, which requires many testing cycles (many hundreds to many thousands depending on the type of component).

The JG-PP Working Group and project technical representatives discussed sample size at length. For those tests where five test vehicles are used, the sample size for each component type would be 25. To achieve a 90% confidence level at 10% cumulative failures, a minimum sample size of 21 is required. The stakeholder's felt that the 25-sample size rather than 32 as specified in IPC-9701 would provide statistically meaningful results. IPC-SM-785, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, has equations for calculating the minimum number of failure-free test cycles for a given cumulative failure probability percentage with sample size and design life cycle requirement.

## 3. TEST DESCRIPTIONS

Section 3 briefly describes those tests that will permit project participants to consider qualifying lead-free solder alloys. Each test description includes a procedure, rationale, test parameters and acceptance criteria. Where appropriate, the descriptions also include the number and type of test specimens per solder alloy, number of trials per specimen, any major or unique equipment, and data recording and calculation requirements.

Section 3.1 describes those auxiliary tests conducted prior to, during, or after each reliability test. Section 3.2 describes each common reliability test listed in Table 4 of Section 2.3. Section 3.3 describes each extended reliability test listed in Table 5 of Section 2.4.

The information contained in Section 3 is brief and is intended to provide the information needed to understand the tests. These sections can serve as a guide to those performing the tests.

### 3.1. Auxiliary Testing

#### 3.1.1. Electrical Continuity Testing

An event detector (Anatech or equivalent conforming to IPC-SM-785) will be used to monitor the electrical continuity of each channel on the test vehicle, and thereby detect solder joint failures that occur during testing (i.e. an "event"). The failure criteria measured by the event detector will be 10 events per channel with an interruption of electrical continuity (≥300 Ω up to 1000 Ω) for periods greater than 0.2 μsec per IPC-SM-785 *(Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments)*.

**Table 6. Electrical Continuity Testing**

| | |
|---|---|
| **Failure Criteria** | • 10 events per channel<br>• 0.2 microsecond<br>• ≥ 300 Ω resistance for thermal shock and thermal cycle<br>• ≥1000 Ω for mechanical shock and vibration |

Major or Unique Equipment
- Event detector (Anatech or equivalent)

Data Recording and Statistical Analysis
- Record of failures

### 3.1.2. Coefficient of Thermal Expansion (CTE) Testing

Measure CTE of SMT components only and the test vehicle per IPC-TM-650, Method 2.4.41 (*Coefficient of Linear Thermal Expansion for Electrical Insulating Materials*). The measured CTE values will be representative of each component as a composite of its construction/configuration.

### 3.1.3. Component Height Testing

The component height off the printed wiring board of each SMT component type will be measured during the microsection examination of the finished vehicle assemblies set aside for post-test inspection (see 2.2.2).

## 3.2. Common Environmental Exposure and Physical Reliability Tests

### 3.2.1. Vibration

Description
This test determines solder joint failures during exposure to vibration conditions.

Perform this test in accordance with MIL-STD-810F *(Test Method Standard for Environmental Engineering Considerations and Laboratory Tests)* Method 514.5, (Vibration) and the following procedure:

- Measure the electrical resistance of each channel prior to testing
- Place the PWAs into a test fixture in random order and mount the test rack onto a vibration table. Expose PWAs to the following vibration profile in each of the three orthogonal axes for one hour per axis:
- Continuously monitor the electrical continuity of the solder joints during the test.
- It is assumed that most failures will occur with the vibration in the axis perpendicular to the plane of the board (Z axis) as a result of board bending. Increase the vibration level in this axis by approximately 2.0 $g_{rms}$ and shake for one hour. Continue to increase the Z axis vibration level in 2.0 $g_{rms}$ increments, shaking for one hour per step until all parts have failed or 20.0 $g_{rms}$ is reached.

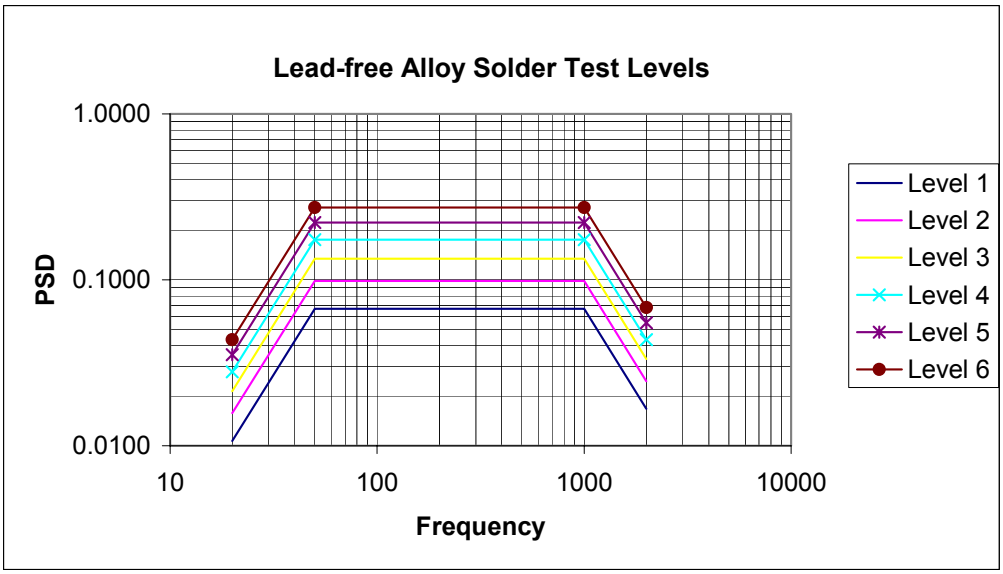



**Figure 4. Vibration Spectrum**

**Table 7. Vibration Profile**

| **Level 1** | **Level 2** | **Level 3** |
|---|---|---|
| 20 Hz @ 0.0107 g²/Hz | 20 Hz @ 0.0157 g²/Hz | 20 Hz @ 0.0214 g²/Hz |
| 20 - 50 Hz @ +6.0 dB/oct | 20 - 50 Hz @ +6.0 dB/oct | 20 - 50 Hz @ +6.0 dB/oct |
| 50 - 1000 Hz @ 0.067 g²/Hz | 50 - 1000 Hz @ 0.0984 g²/Hz | 50 - 1000 Hz @ 0.134 g²/Hz |
| 1000 - 2000 Hz @ -6.0 dB/oct | 1000 - 2000 Hz @ -6.0 dB/oct | 1000 - 2000 Hz @ -6.0 dB/oct |
| 2000 Hz @ 0.0167 g²/Hz | 2000 Hz @ 0.0245 g²/Hz | 2000 Hz @ 0.0334 g²/Hz |
| Composite = 9.9 $g_{rms}$ | Composite = 12.0 $g_{rms}$ | Composite = 14.0 $g_{rms}$ |
| **Level 4** | **Level 5** | **Level 6** |
| 20 Hz @ 0.0279 g²/Hz | 20 Hz @ 0.0354 g²/Hz | 20 Hz @ 0.0437 g²/Hz |
| 20 - 50 Hz @ +6.0 dB/oct | 20 - 50 Hz @ +6.0 dB/oct | 20 - 50 Hz @ +6.0 dB/oct |
| 50 - 1000 Hz @ 0.175 g²/Hz | 50 - 1000 Hz @ 0.2215 g²/Hz | 50 - 1000 Hz @ 0.2734 g²/Hz |
| 1000 - 2000 Hz @ -6.0 dB/oct | 1000 - 2000 Hz @ -6.0 dB/oct | 1000 - 2000 Hz @ -6.0 dB/oct |
| 2000 Hz @ 0.0436 g²/Hz | 2000 Hz @ 0.0552 g²/Hz | 2000 Hz @ 0.0682 g²/Hz |
| Composite = 16.0 $g_{rms}$ | Composite = 18.0 $g_{rms}$ | Composite = 20.0 $g_{rms}$ |

Rationale

The JG-PP stakeholders felt that MIL-STD-810F, Method 514.5, (Vibration) would be a reliable indication of lead-free solder alloys unsuited to endure dynamic mechanical forces. The vibration test will be run in accordance with the vibration spectrum in Figure 4 developed specifically for this JG-PP project by the Electronic, Electrical and Electromechanical (EEE) Parts and Packaging Group of NASA Marshall Space Flight Center. Project stakeholders agreed that a stepwise vibration

spectrum covering a wide array of intensities would best meet the specifications required by the lead-free solder project consortium.

**Table 8. Vibration Test Methodology**

| | |
|---|---|
| **Parameters** | • 1 hour per axis<br>• Start at 9.9 $g_{rms}$ in all three axes, then step up in 2 $g_{rms}$ increments in the Z axis |
| **Number and Type of Specimens** | 5 PWAs per solder alloy |
| **Trials per Specimen** | 1 |
| **Acceptance Criteria** | Electrical reliability better than or equal to tin/lead controls |

Major or Unique Equipment
- Vibration table
- Event detector (Anatech or equivalent)
- Fixture

Data Recording and Calculations
- Record data and compare to acceptance criteria as specified in JTP Section 3.1.1.

### 3.2.2. Mechanical Shock

Description
The purpose of this test is to determine the resistance of the solder to the stresses associated with high-intensity shocks induced by service environments. Tests will be performed to meet the requirement specified in MIL-STD-810F. Shock requirement for other applications will be established by incremental increase of shock level with specific shock numbers until failures of the most assemblies.

Perform this test in accordance with MIL-STD-810F, Method 516.5, (Shock), except where noted. Mount the PWAs to an electro-dynamic shaker. Program the required shock response spectrum (SRS) into the digital shock controller. The digital controller will generate a transient shock time history satisfying the maximum SRS requirement. Two sets of test vehicles will undergo mechanical shock testing:
- Test Set #1 follows the requirements set by MIL-STD-810F, Method 516.5 (see Figure 5 and Table 9): Apply three (3) shock transients in each direction along each of the three orthogonal axes. This test will be conducted for three test shock response spectra as specified in the specification:
- Functional Test for Flight Equipment

- Functional Test for Ground Equipment
- Crash Hazard Test for Ground Equipment

  Following completion of the three shock transients in each direction along each of the three orthogonal axes for the Crash Hazard Test for Ground Equipment, repeat the test using 100 shock transients in each direction along each of the 3 orthogonal axes for the Crash Hazard Test for Ground Equipment.

- Test Set #2 partially follows MIL-STD-810F, Method 516.5, but calls for higher shock amplitudes (g's) (see Figure 6 and Table 10): Apply the shock transients 100 times only in the Z-axis normal to the plane of the board at the MIL-STD-810F, Method 516.5 Functional Test for Flight Equipment, Functional Test for Ground Equipment, and Crash Hazard Test for Ground Equipment levels. Increase step-wise the g level and apply shock only in the Z-direction specified in Table 2. Both shock level steps and crossover frequencies may be required to be modified based on the initial "pathfinder" test sample. Continue test until failure of a majority (greater than 63 percent) of assemblies is observed.

Prior to the above testing, an extra "pathfinder" board will be subjected to both test conditions in order to identify potential problems with the test setup as well as better define g levels and number of shocks defined in Table 10. The resulting test SRS shall be within +3dB and -1.5dB of the nominal requirement over a minimum of 90% of the frequency band when using a 1/12-octave analysis bandwidth. The remaining 10% of the frequency band shall be within +6dB and -3dB of the nominal requirement. Continuously monitor the electrical continuity of the solder joints during the test. Record the results. (Note: It is recognized that in a laboratory environment, the supplied SRS is very difficult to meet at low frequencies due to the large displacements involved. Therefore, the low frequency cutoff of the SRS may be defined as the first natural frequency of the test item minus one octave.)

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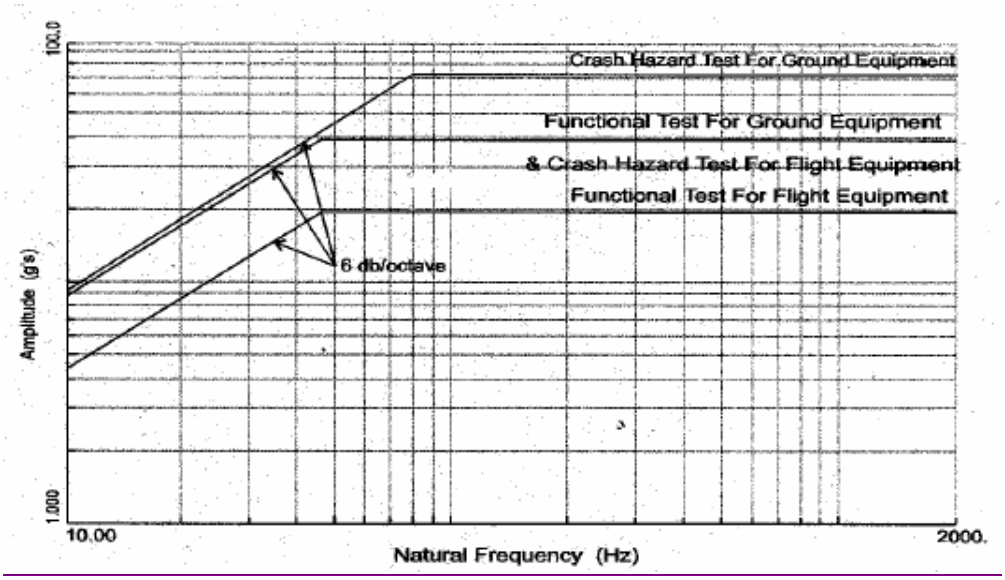


*Source*: MIL-STD-810F, Method 516.5

**Figure 5. Mechanical Shock Response Spectrum – Test Set #1**

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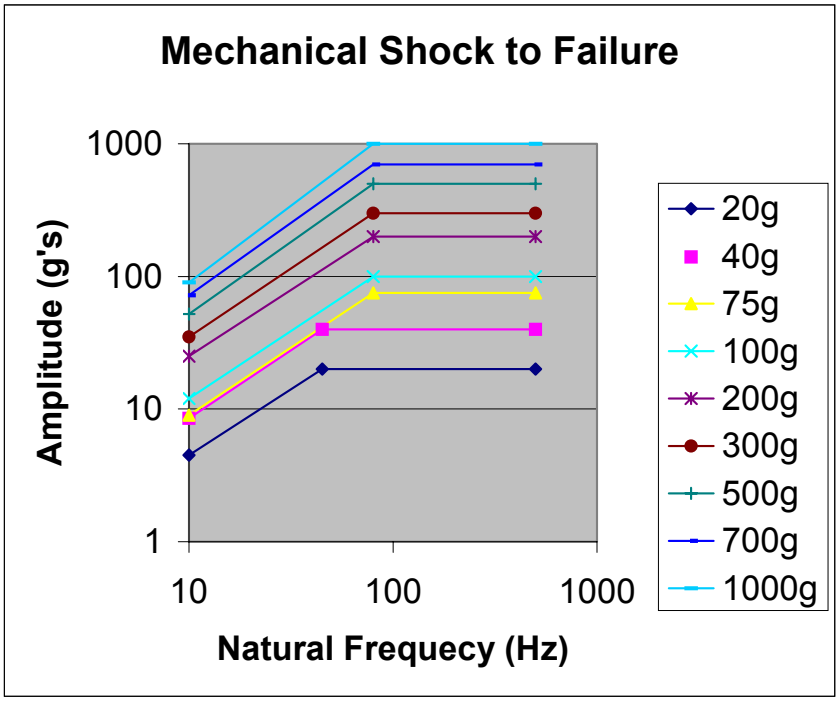


**Figure 6. Mechanical Shock Response Spectrum – Test Set #2**

Rationale

The JG-PP stakeholders felt that MIL-STD-810F, Method 516.5, Procedure I (Functional Shock) would be a reliable indication of solders that are unsuited to endure the high-intensity shocks associated with service use.

The stakeholders agreed to the need for two test sets representing different shock scenarios. The first set addresses the exact requirements that many military customers have to see data correlating to a long-standing military specification. MIL-STD-810F, Method 516.5, Procedure I (Functional Shock) is intended to test materiel (including mechanical, electrical, hydraulic, and electronic) in its functional mode and to assess the physical integrity, continuity and functionality of the materiel to shock. In general, the materiel is required to function during the shock and to survive without damage to shocks representative of those that may be encountered during operational service.

A prior shock spectrum had been considered, as early as December 2001, but after close examination it was determined that the spectrum was not feasible for our testing because current test vehicle is much too large to be tested under the originally purposed mechanical shock profile. The original profile was established to test actual assembled components and packages, which would be much smaller. Therefore, new profiles were researched, discussed and now appear in the JTP.

The project representatives agreed that all three shock levels (Functional Test for Flight Equipment, Functional Test for Ground Equipment, and Crash Hazard Test for Ground Equipment) should be tested, if feasible, because of the different conditions (and defense and space hardware) they correspond to.

For test set one, project representatives felt that going above and beyond MIL-STD-810F by increasing the number of shock transients, from 3 to 100 in each direction along each of the 3 orthogonal axes for the Crash Hazard Test for Ground Equipment would maximize failure mechanisms providing excellent data for analysis.

The second test set will characterize mechanical shock resistance of various technologies for a harsher environment covering many application specific scenarios for industry and not covered by military specification. The test is intended to mechanically shock the boards to obtain as many failures as possible. Shock will be performed only in the Z-axis to minimize confounding failure mechanisms. The various shock levels in Test Set #2 were suggested by NASA Jet Propulsion Laboratory, March 2004, and agreed to by the other project stakeholders. The first three

shock scenarios (Functional Test for Flight Equipment, Functional Test for Ground Equipment, and Crash Hazard Test for Ground Equipment) mirror those in Test Set #1 except they are being applied in all three axes (instead of one axis). The next six levels were derived by the NASA JPL representative based on review of limited published data showing under what conditions significant failures might be achieved. In addition, MIL-STD-810F was considered as baseline with inclusion of partial fatigue effect and test methodology proposed for the IPC 9703 using step-wise increase in g level till failure in order to cover many applications.

Running two test sets—one in all axes but at reduced number of shocks and amplitude, and the other in one axis at higher numbers of shocks and amplitude—will ensure that whatever axis is the primary failure mode will be covered by the test plan. Furthermore, Test Set #2 conditions will increase the likelihood that significant (greater than 63 percent) parts failure will be achieved, thus enabling statistical (e.g., Weibull) plots to be generated and allowing for better delineation between the performance of different solder alloys than Test Set #1 alone might allow.

**Table 9. Mechanical Shock Test Methodology – Test Set #1**

Deleted: Table 5. Mechanical Shock Methodology

<table>
<tr><td>Parameters</td><td colspan="9">• Apply three shock transients (Figure 1) in each direction along each of the 3 orthogonal axes for three test shock response spectra</td></tr>
<tr><td></td><td>Test Shock Response Spectra</td><td>Initial G</td><td>Slope</td><td>Peak G</td><td>Ts (ms)</td><td>Cross-Over Freq</td><td>Z-Axis</td><td>X-Axis</td><td>Y-Axis</td></tr>
<tr><td></td><td>Functional Test for Flight Equipment</td><td>4.5</td><td>6</td><td>20</td><td>15-23</td><td>45</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td></td><td>Functional Test for Ground Equipment</td><td>8.5</td><td>6</td><td>40</td><td>15-23</td><td>45</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td></td><td>Crash Hazard Test for Ground Equipment</td><td>9</td><td>6</td><td>75</td><td>8-13</td><td>80</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td></td><td>Crash Hazard Test for Ground Equipment</td><td>9</td><td>6</td><td>75</td><td>8-13</td><td>80</td><td>100</td><td>100</td><td>100</td></tr>
<tr><td>Number and Type of Specimens</td><td colspan="9">• 2 PWAs per solder alloy for Test Set #1<br>• One “pathfinder” board</td></tr>
<tr><td>Acceptance Criteria</td><td colspan="9">• Electrical continuity better than or equal to tin/lead controls</td></tr>
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**Table 10. Mechanical Shock Test Methodology – Test Set #2**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameters** | • Apply the shock transients (Figure 2) in one axis parallel to the plane of the board, in a step-wise function, until a majority (≥ 63%) of all parts fail | | | | | | |
| | Test Shock Response Spectra | Initial G | Slope | Peak G | Ts (ms) | Cross-Over Freq | Z-Axis |
| | Functional Test for Flight Equipment | 4.5 | 6 | 20 | 15-23 | 45 | 100 |
| | Functional Test for Ground Equipment | 8.5 | 6 | 40 | 15-23 | 45 | 100 |
| | Crash Hazard Test for Ground Equipment | 9 | 6 | 75 | 8-13 | 80 | 100 |
| | Level 1 | 12 | 6 | 100 | 15-23 | 80(1) | 100 |
| | Level 2 | 25 | 6 | 200 | 15-23 | 80(1) | 100 |
| | Level 3 | 35 | 6 | 300 | 15-23 | 80(1) | 100 |
| | Level 4 | 52 | 6 | 500 | 15-23 | 80(1) | 100 |
| | Level 5 | 72 | 6 | 700 | 15-23 | 80(1) | 100 |
| | Level 6 | 90 | 6 | 1000 | 15-23 | 80(1) | 100(2) |
| **Number and Type of Specimens** | • 2 PWAs per solder alloy for Test Set #2<br>• One "pathfinder" board | | | | | | |
| **Acceptance Criteria** | • Electrical continuity better than or equal to tin/lead controls | | | | | | |
| **NOTE** | • (1) Cross-over frequency may change depending on resonant frequency<br>• (2) It may be necessary to go above 100 shocks to achieve the required failure rate (>63%) | | | | | | |

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Major or Unique Equipment

- Shock table
- Event detector (Anatech or equivalent)
- Fixture

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP Section 3.1.1.

### 3.2.3. Thermal Shock

Description
This test determines a test specimen's resistance to degradation from thermal shock.

Perform this test in accordance with MIL-STD-810F, Method 503.4, Procedure I (Temperature Shock Steady State) and the following:

- Continuously monitor the electrical continuity of the solder joints during the test.
- Cycle from -55 to +125°C for 1000 cycles.

Rationale
The JG-PP stakeholders felt that MIL-STD-810F, Method 503.4, Procedure I (Temperature Shock Steady State) would be a reliable indication of lead free solder alloys that are unsuited to endure the high-intensity thermal shock associated with service use.

**Table 11. Thermal Shock Test Methodology**

| | |
|---|---|
| **Parameters** | • -55°C to +125°C<br>• 1000 shock cycles<br>• 10 sec, max transfer<br>• 15 minutes, dwell |
| **Number and Type of Specimens** | 5 PWAs per solder alloy |
| **Trials per Specimen** | 1 |
| **Acceptance Criteria** | Electrical reliability better than or equal to tin/lead controls |

Major or Unique Equipment
- Event detector (Anatech or equivalent)
- Dual Thermal shock chamber

Data Recording and Calculations
- Record data and compare to acceptance criteria as specified in JTP Section 3.1.1.

### 3.2.4. Thermal Cycling

Description
This test determines a test specimen's resistance to degradation from thermal cycling.

Perform this test in accordance with IPC-SM-785 *(Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments)* and the following procedure.

- Continuously monitor the electrical continuity of the solder joints during the test. Place one set of PWAs in thermal chamber at -55 ºC to +125ºC. Cycle until 63% failures achieved.
- Place another set of PWAs in thermal chamber at -20 ºC to +80 ºC. Cycle until 63% failures achieved.

**Table 12. Thermal Cycling Test Methodology**

| | |
|---|---|
| **Parameters, Manufactured PWAs** | • -55°C to +125°C<br>• -20°C to 80°C<br>• Cycles: Until 63% failures or greater<br>• Decision point at 5000 cycles if 63% failure not yet achieved<br>• 5 to 10°C/minute ramp<br>• 30 minute high temperature dwell<br>• 10 minute low temperature dwell |
| **Parameters, Rework PWAs** | • -55°C to +125°C<br>• Cycles: Until 63% failures or greater<br>• Decision point at 5000 cycles if 63% failure not yet achieved<br>• 5 to10°C/minute ramp<br>• 30 minute high temperature dwell<br>• 10 minute low temperature dwell |
| **Number and Type of Specimens** | 5 PWAs per solder alloy |
| **Trials per Specimen** | 1 |
| **Acceptance Criteria** | Electrical reliability better than or equal to tin/lead controls |

Rationale

Technical representatives from the U.S. Army Aviation and Missile Command (AMCOM) noted that they required enough temperature cycles to produce sufficient failures for statistical analysis. In addition, two temperature ranges are required in order to define acceleration factors to allow extrapolation of the data to their systems' actual use conditions. AMCOM proposed temperature-cycling ranges of -55°C to +125°C and -20°C to +80°C. Although 1,000 temperature cycles may be enough for some Programs to certify a product, this will not result in enough component failures for valid statistical analysis.

After examining the available data on dwell time effect, the lead-free solder project participants reached agreement that the high-temperature dwell time for the -20 to +80°C and -55°C to +125°C thermal cycles will be increased to 30 minutes. Solder alloy creep during the high temperature dwell of the thermal cycle is largely responsible for damage within the solder joints. In order to maximize the effects of solder alloy creep, a 30-minute high temperature dwell will be used for this project.

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Major or Unique Equipment

- Event detectors (Anatech or equivalent)
- Two thermal cycle chambers

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP Section 3.1.1.

### 3.2.5. Combined Environments Test

Description

This test determines the operational and endurance limits of the PWAs (test vehicles) and solder alloys.

The Combined Environments Test (CET) for the JG-PP Pb-Free Solder Project is based on a modified Highly Accelerated Life Test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process.

The CET process can identify design and process related problems in a much shorter time frame than other development tests. In this project, CET will determine the operation and endurance limits of the solder alloys by subjecting the test vehicles to accelerated environments. The limits identified in CET will be used to compare performance differences in the Pb-free test alloys vs. the baseline standard Sn/Pb (63/37) alloy. The primary accelerated environments are temperature extremes (both limits

and rate of change) and vibration (pseudo-random six degrees of freedom [DOF]) used in combination.

Perform this test in accordance with the following procedure:

- Perform this test utilizing a temperature range of –55 to 125°C with 20°C/minute ramps. The dwell times at each temperature extreme are the times required to stabilize the test sample plus a 15-minute soak. 10 $g_{rms}$ pseudo-random vibration is applied for the last 10 minutes of the cold and hot soaks. Testing is continued until sufficient data is generated to obtain statistically significant Weibull plots indicating relative solder joint endurance (cycles to failure) rates. If significant failure rates are not evidenced after 100 cycles, the vibration levels are incremented by 5 $g_{rms}$ and cycling continued for an additional 100 cycles. This process is repeated until all parts have failed or 20 $g_{rms}$ is reached.

  Rationale
  The JG-PP stakeholders felt that Combined Environments Testing would provide a method to identify comparative potential reliability differences in the test alloys vs. the Sn/Pb baseline in a short period of time.

**Table 13. Combined Environments Test Methodology**

| | |
|---|---|
| **Parameters** | • -55 to 125°C<br>• 20°C/minute ramp<br>• 15 minute soak<br>• 10 $g_{rms}$ |
| **Number and Type of Specimens** | 5 PWAs per solder alloy |
| **Trials per Specimens** | 1 |
| **Acceptance Criteria** | Electrical reliability better than or equal to tin/lead controls |

Major or Unique Equipment
- HALT chamber
- Event detector (Anatech or equivalent)
- Fixturing

Data Recording and Calculations
- Record data and compare to acceptance criteria as specified in JTP Section 3.1.1.

## 3.3. Extended Testing Procedures

### 3.3.1. Salt Fog

Description

This test determines the effects of salt deposits on the physical and electrical aspects of lead-free solder joints.

Perform this test in accordance with MIL-STD-810F, Method 509.4 (Salt Fog) and the following procedure:

- Measure and record the electrical resistance of each channel before salt fog exposure
- Place test PWAs in salt fog chamber
- Use a 5 +/- 1% salt solution concentration.
- Standard exposure of 48 hours of exposure and 48 hours of drying time; alternate 24-hour periods of salt fog exposure and drying conditions for a minimum of four 24 hour periods (two wet and two dry).
- Temperature in the exposure zone should be maintained at 35 +/- 2$^{o}$C (94 +/- 4$^{o}$F).
- Measure and record the electrical resistance of each channel after exposure
- Rinse PWA per MIL-STD-810F, Method 509.4 (Salt Fog) and inspect visually for corrosion.

Rationale

Technical representatives from the Air Force F-15 program and Naval Air Warfare Center Weapons Division require salt fog per MIL-STD-810F Method 509.4 (Salt Fog) (or equivalent) because this test simulates the coastal atmosphere to which U.S. Air Force and Navy aircraft are subjected. The salt fog test validates the effect/non-effect of corrosion on the external package elements (leads). This is both a mechanical and electrical effect. Since we will be using a lead free-lead finish, these representatives want to know the effect.

**Table 14. Salt Fog Methodology**

| | |
|---|---|
| **Parameters** | • 5 +/- 1% salt solution concentration<br>• Four 24 hour periods (two wet and two dry)<br>• Exposure zone temperature 35 +/- 2$^{o}$C |
| **Number and Type of Specimens** | 3 PWAs per solder alloy |

| | |
|---|---|
| **Trials per Specimen** | 1 |
| **Acceptance Criteria** | Performs better than or equal to tin/lead controls |

Major or Unique Equipment
- Salt fog chamber

Data Recording and Calculations
- Record the electrical resistance of each channel both pre and post execution of the salt fog test
- Record data, under 10X-20X magnification and compare to visual failure criteria for solder joints including:
  - Pitting
  - Flaking
  - Blistering
  - Other corrosion characteristics

### 3.3.2. Humidity

Description
This test determines a test specimen's resistance to the deteriorative effects of high humidity and heat conditions.

Perform this test in accordance with MIL-STD-810F, Method 507.4, (Humidity) and the following procedure:

- Measure and record the electrical resistance of each channel before humidity exposure
- Install test vehicle in the test chamber in the required configuration, adjust temperature to 23 +/- 2$^{o}$C and 50 +/- 5% relative humidity and maintain for 24 hours.
- Adjust the test chamber temperature to 30$^{o}$C and the RH to 95%.
- Run test for five 48-hour cycles per Figure 507.4-1 in MIL-STD-810F, Method 507.4 (Humidity).
- Measure and record the electrical resistance of each channel after testing.

Rationale
Technical representatives from the Air Force F-15 program, and Naval Air Warfare Center Weapons Division require humidity testing per MIL-STD-810F Method 507.4 (Humidity) (or equivalent). The humidity (moisture resistance) test is required to evaluate, in an accelerated manner, the effect of high humidity and high temperature environments (i.e., tropical environment) on the lead-free solder joint appearance.

**Table 15. Humidity Test Methodology**

| | |
|---|---|
| **Parameters** | • Five 48-hour cycles per Figure 507.4-1 in MIL-STD-810F, Method 507.4 (Humidity) |
| **Number and Type of Specimens** | 3 PWAs per solder alloy |
| **Trials per Specimens** | 1 |
| **Acceptance Criteria** | Performs better than or equal to tin/lead controls |

Major or Unique Equipment
- Temperature-humidity chamber

Data Recording and Calculations
- Record the electrical resistance of each channel both pre and post execution of the humidity test
- Record data, under 10X-20X magnification and compare to visual failure criteria for solder joints including:
  - Pitting
  - Flaking
  - Blistering
  - Other corrosion characteristics

### 3.3.3. Surface Insulation Resistance (SIR)

Description
This test method is to characterize the test vehicle assembly process by determining the degradation of electrical insulation resistance of the lead-free test vehicle after exposure to the specified process. This test is carried out at high humidity and heat conditions.

Perform this test in accordance with IPC-TM-650, Method 2.6.3.3 (Surface Insulation Resistance, Fluxes) and the following procedure:

- Test performed independently
- Process IPC-B-24 boards per Table 16. Surface Insulation Resistance Test Methodology

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Rationale

Technical representatives from Naval Air Warfare Center Weapons Division require Surface Insulation Resistance testing to demonstrate the relative degree to which the lead-free test vehicle is susceptible to dendritic growth due to the presence of condensed moisture. The concern is because eliminating all moisture containing environments from the test matrix may lead to questions regarding basic performance at the end of the study. For example, were there anomalous results with "standard" processing and "representative" configurations in a moist environment? The lead dendrite problem found with the citric acid flux conversion is one example. As such, the SIR test method is particularly suitable for PWA manufacturing process control.

**Table 16. Surface Insulation Resistance Test Methodology**

| | |
|---|---|
| **Parameters** | • 85 +/- 2°C at 85 +/- 2% relative humidity for 168 hours. |
| **Number and Type of Specimens** | IPC-B-24 boards<br>6 – Boards with SnAgCu reflow solder alloy and flux<br>6 – Boards with SnAgCuBi reflow solder alloy and flux<br>6 – Boards with SnPb reflow solder alloy and flux<br>6 – Boards with SnCu wave solder alloy and flux<br>6 – Boards with SnAgCu wave solder alloy and flux<br>6 – Boards with SnPb wave solder alloy and flux<br>6 – Boards with bare copper finish, no solder paste, only processed through cleaning procedures<br>5 – Boards with bare copper finish, no solder paste, passed through reflow and wave solder machines then cleaned |
| **Trials per Specimens** | 1 |
| **Acceptance Criteria** | $\geq 10^8\ \Omega$ |

Major or Unique Equipment

- IPC-B-24 boards
- Temperature-humidity chamber
- Surface Insulation Resistance (SIR) test setup

Data Recording and Calculations

- Record data, including fluxes in use and the manufacturing and cleaning methods employed, and compare to acceptance criteria as specified in IPC-TM-650, Method 2.6.3.3 (Surface Insulation Resistance, Fluxes).
- Record data and compare to visual pass/fail criteria per IPC-TM-650, Method 2.6.3.3 (Surface Insulation Resistance, Fluxes)

### 3.3.4. Electrochemical Migration Resistance Test

Description
This test is used to provide a means to assess surface electrochemical migration on the no-lead solder test vehicles.

Perform this test in accordance with IPC-TM-650, Method 2.6.14.1 (Electrochemical Migration Resistance Test) and the following procedure:

- Test performed independently
- Process IPC-B-25A boards, "D-comb pattern" per Table17. Electrochemical Migration Resistance Test Methodology

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Rationale
Technical representatives from Naval Air Warfare Center felt that electrochemical migration is a real and reasonably possible failure mode with any new alloy.

**Table 17. Electrochemical Migration Resistance Test Methodology**

| | |
|---|---|
| **Parameters** | One of the following temperature ranges:<br>• 40°C +/- 2°C at 93% +/- 2% RH,<br>• 65°C +/- 2°C at 88.5% +/- 3.5% RH<br>• 85°C +/- 2°C at 88.5% +/- 3.5% RH,<br>depending on the flux used |
| **Number and Type of Specimens** | IPC-B-25A boards with D-comb pattern<br>6 – Boards with SnAgCu reflow solder alloy and flux<br>6 – Boards with SnAgCuBi reflow solder alloy and flux<br>6 – Boards with SnPb reflow solder alloy and flux<br>6 – Boards with SnCu wave solder alloy and flux<br>6 – Boards with SnAgCu wave solder alloy and flux<br>6 – Boards with SnPb wave solder alloy and flux<br>6 – Boards with bare copper finish, no solder paste, only processed through cleaning procedures<br>5 – Boards with bare copper finish, no solder paste, passed through reflow and wave solder machines then cleaned |
| **Trials per Specimens** | 1 |
| **Acceptance Criteria** | • $IR_{final} \geq (IR_{initial})/10$, that is the average insulation resistance shall not degrade by more than one decade as a result of the applied bias.<br>• No evidence of electrochemical migration (filament growth) that reduces the conductor spacing by more than 20%<br>• No corrosion of the conductors; minor discoloration of one polarity of the comb pattern conductors is normal. |

Major or Unique Equipment

- IPC-B-25A boards
- Temperature-humidity chamber
- Electrochemical Migration Resistance test setup

Data Recording and Calculations

- Record data, including fluxes in use and the manufacturing and cleaning methods employed, and compare to acceptance criteria as specified in IPC-TM-650, Method 2.6.14.1 (Electrochemical Migration Resistance Test).
- Record data and compare to visual pass/fail criteria per IPC-TM-650, Method 2.6.14.1 (Electrochemical Migration Resistance Test)

## 4. REFERENCE DOCUMENTS

Table 18 summarizes the documents referenced in this JTP.

**Table 18. Reference Documents**

| Reference Document | Title | Date | Applicable Section(s) of Reference Document | JTP Topic | JTP Section |
|---|---|---|---|---|---|
| ANSI/J-STD-003 | Solderability Tests for Printed Boards | Apr 92 | 4.3.1 | Assembly Criteria | 2.1. |
| IPC/EIA J-STD-001 Revision C | Requirements for Soldered Electrical and Electronic Assemblies | Oct 96 | All | Assembly Criteria | 2.1. |
| IPC-A-.610 | Acceptability for Electronic Assemblies | Jan 00 | Section 6, Soldering Acceptability Requirements, Section 7, Cleanliness | Assembly Workmanship | 2.1. |
| IPC-2221 | Generic Standard on Printed Board Design | Not Dated | All | Assembly Criteria | 2.1. |
| IPC-2222 | Sectional Design Standard for Rigid Organic Printed Boards | Not Dated | All | Assembly Criteria | 2.1. |
| IPC-6012 | Qualification and Performance Specification for Rigid Printed Boards | July 00 | All | Assembly Workmanship | 2.1. |
| IPC-9201 | Surface Insulation Handbook | July 96 | Cyclical Test Environments | Humidity | 3.3.2. |
| IPC-9701 | Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments | Jan 02 | Section 3.4.2, Cyclic Temperature Range/Swing Section 4.2.2.1, Test Board Design Requirements | Board Design, Thermal Cycle | 2.1. and 3.2.4. |
| IPC-SM-785 | Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments | Nov 92 | All | Thermal Cycling | 3.2.4. |
| IPC-TM-650, Method 2.4.41 | Coefficient of Linear Thermal Expansion for Electrical Insulating Materials | Mar 86 | All | Coefficient of Thermal Expansion (CTE) Testing | 3.1.2 |

| Reference Document | Title | Date | Applicable Section(s) of Reference Document | JTP Topic | JTP Section |
|---|---|---|---|---|---|
| IPC-TM-650, Method 2.6.14.1 | Electrochemical Migration Resistance Test | Sept 00 | IPC-TM-650, Method 2.6.14.1 | Electrochemical Migration Resistance Test | 3.3.4. |
| IPC-TM-650, Method 2.6.3.3 | Surface Insulation Resistance, Fluxes | Jan 95 | IPC-TM-650, Method 2.6.3.3 | Surface Insulation Resistance, Fluxes | 3.3.3. |
| MIL-STD-810F | Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Vibration | Jan 00 | Method 514.5 | Vibration | 3.2.1. |
| MIL-STD-810F | Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Shock | Jan 00 | Method 516.5 | Mechanical Shock | 3.2.2. |
| MIL-STD-810F | Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Humidity | Jan 00 | Method 507.4 | Humidity | 3.3.2. |
| MIL-STD-810F | Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Shock | Jan 00 | Method 503.4 | Thermal Shock | 3.2.3. |
| MIL-STD-810F | Test Method Standard for Environmental Engineering Consideration and Laboratory Tests, Salt Fog | Jan 00 | Method 509.4 | Salt Fog | 3.3.1. |